N-Channel 60–V (D–S) Reduced Qgd, Fast Switching WFET®

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ)
60	0.0078 @ V_{GS} = 10 V	30	55
	0.009 @ V_{GS} = 6 V	30	

FEATURES

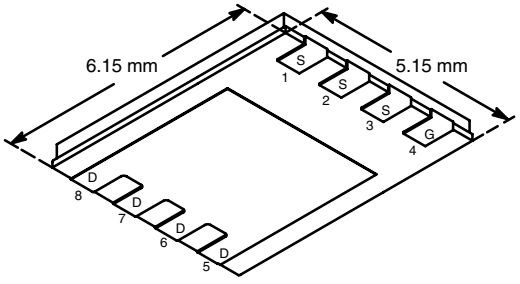
- Extremely Low Q_{gd} WFET Power MOSFET Technology for minimal Switching Losses
- Low Thermal Resistance PowerPAK® package
- 100% R_g and Avalanche Tested

Pb-free
RoHS COMPLIANT

APPLICATIONS

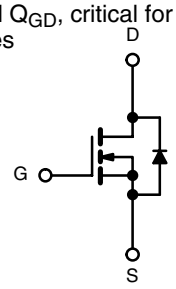
- Primary Side Switch
  - Very Low R_G and Q_{GD}, critical for minimizing Losses

PowerPAK SO-8



Bottom View

Ordering Information: Si7138DP-T1–E3 (Lead (Pb)–free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	30	A
	T_C = 70°C		30	
	T_A = 25°C		19.7[b, c]	
	T_A = 70°C		15.7[b, c]	
Pulsed Drain Current		I_{DM}	80	
Continuous Source-Drain Diode Current	T_C = 25°C	I_S	30[a]	
	T_A = 25°C		4.5[b, c]	
Avalanche Current	L = 0.1mH	I_{AS}	43	A
Single Pulse Avalanche Energy		E_{AS}	93	mJ
Maximum Power Dissipation	T_C = 25°C	P_D	96	W
	T_C = 70°C		61.5	
	T_A = 25°C		5.4[b, c]	
	T_A = 70°C		3.5[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 sec	R_{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 sec
d. See Solder Profile (http://www.vishay.com/doc?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 65 °C/W.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 1 mA	60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA		60.5		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			–8.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2		4	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55°C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 19.7 A		0.0065	0.0078	Ω
		V_{GS} = 6 V, I_D = 18 A		0.0073	0.009	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 19.7 A		84		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		6900		pF
Output Capacitance	C_{oss}			470		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 19.7 A		90	135	nC
		V_{DS} = 30 V, V_{GS} = 6 V, I_D= 19.7 A		55	83	
Gate-Source Charge	Q_{gs}			27.5		
Gate-Drain Charge	Q_{gd}			11		
Gate Resistance	R_g	f = 1 MHz		0.6	0.9	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 3 Ω I_D ≅ 10 A, V_{GEN} = 6 V, R_g = 1 Ω		47	70	ns
Rise Time	t_r			120	180	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 3 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		25	40	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25°C			30	A
Pulse Diode Forward Current[a]	I_{SM}				80	
Body Diode Voltage	V_{SD}	I_S = 2.7 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, di/dt = 100 A/μs, T_J = 25°C		45	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			80	120	nC
Reverse Recovery Fall Time	t_a			30		ns
Reverse Recovery Rise Time	t_b			15		

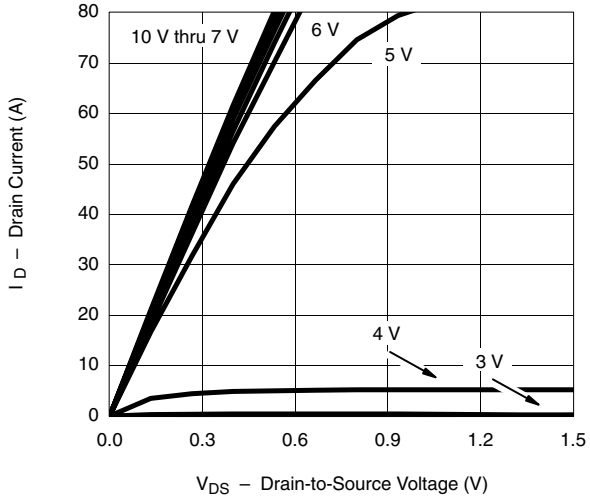
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

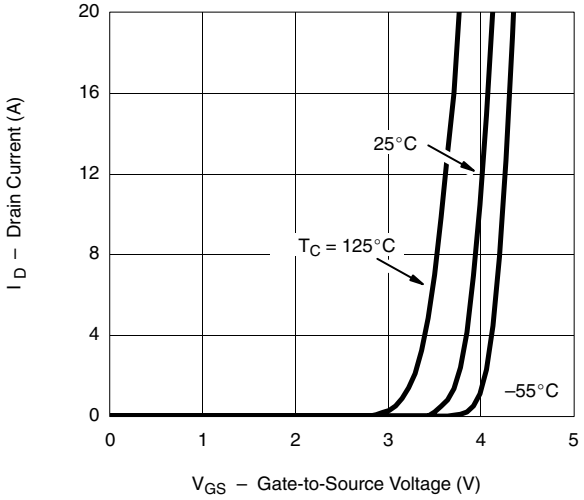
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

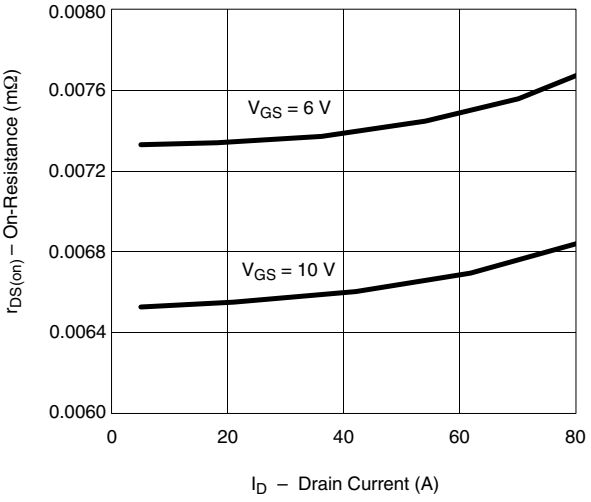
Output Characteristics



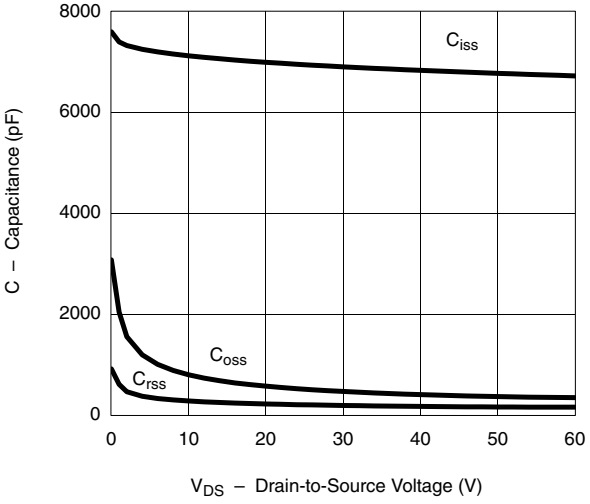
Transfer Characteristics



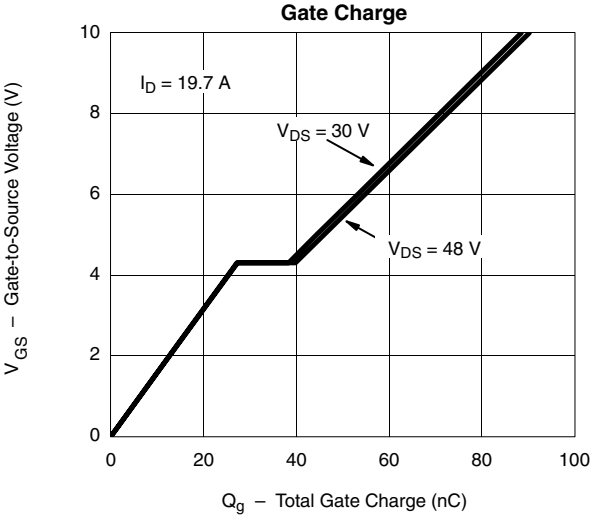
On-Resistance vs. Drain Current and Gate Voltage



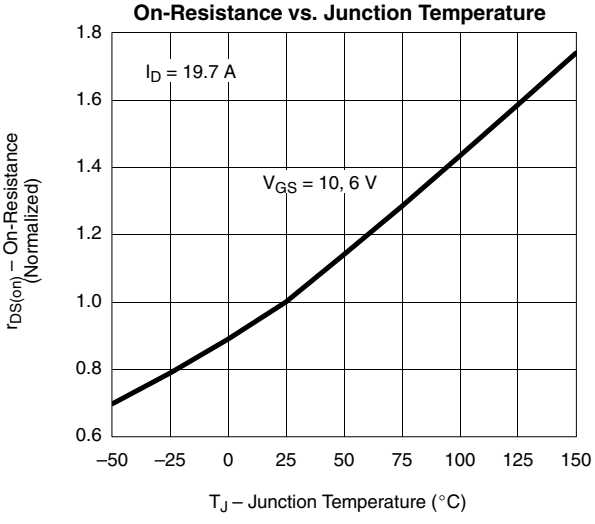
Capacitance



Gate Charge

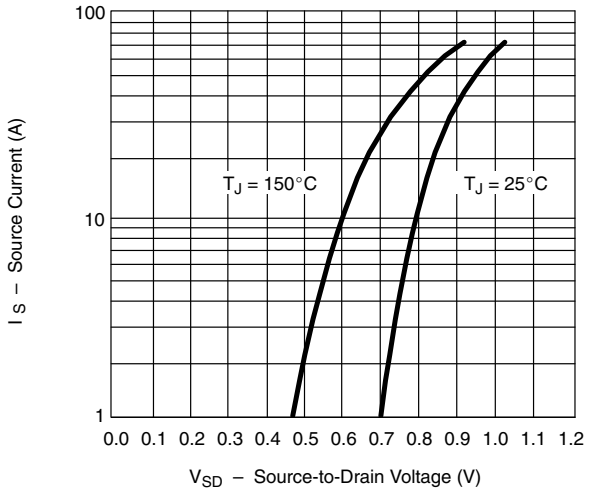


On-Resistance vs. Junction Temperature

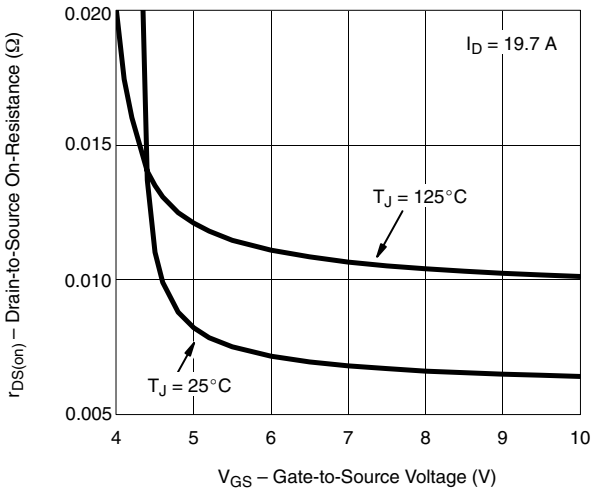


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

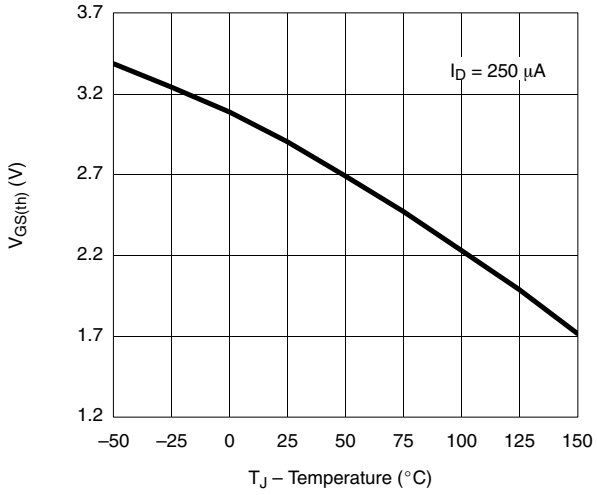
Source-Drain Diode Forward Voltage



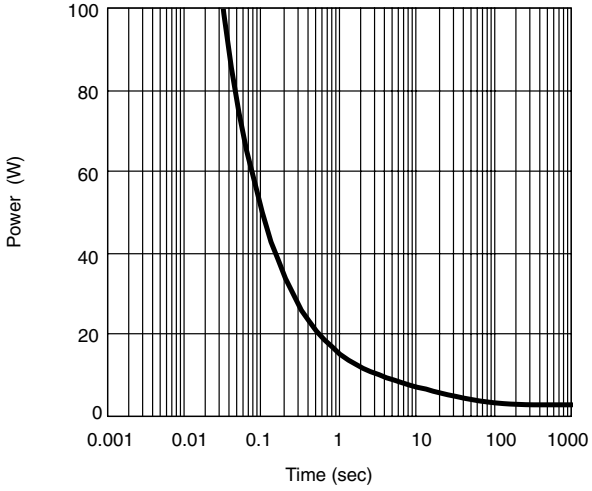
On-Resistance vs. Gate-to-Source Voltage



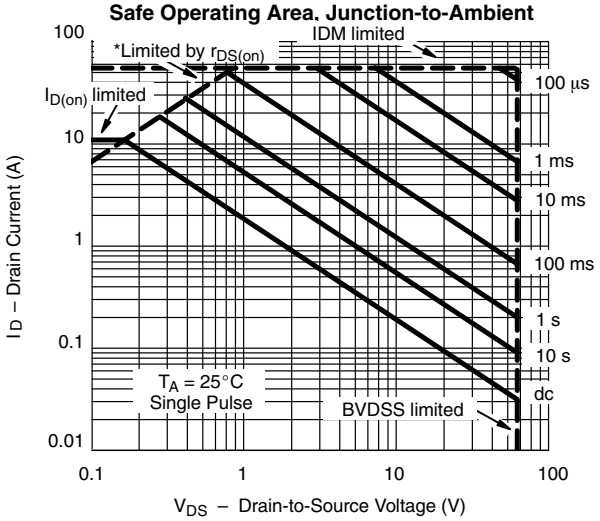
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

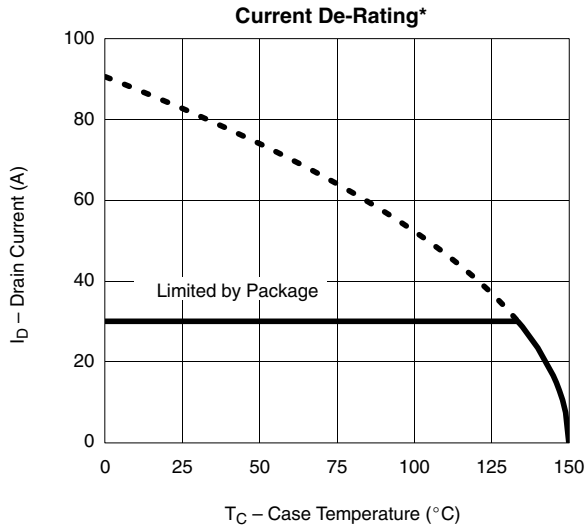


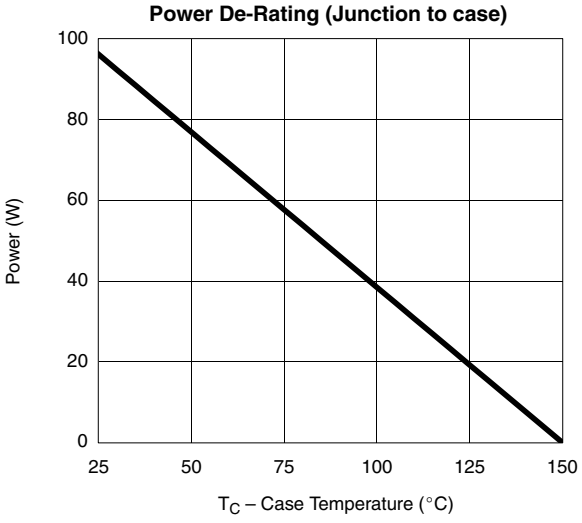
Safe Operating Area, Junction-to-Ambient

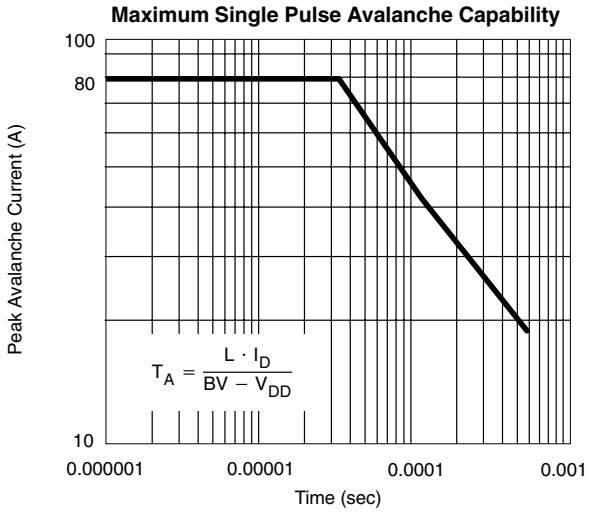


*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



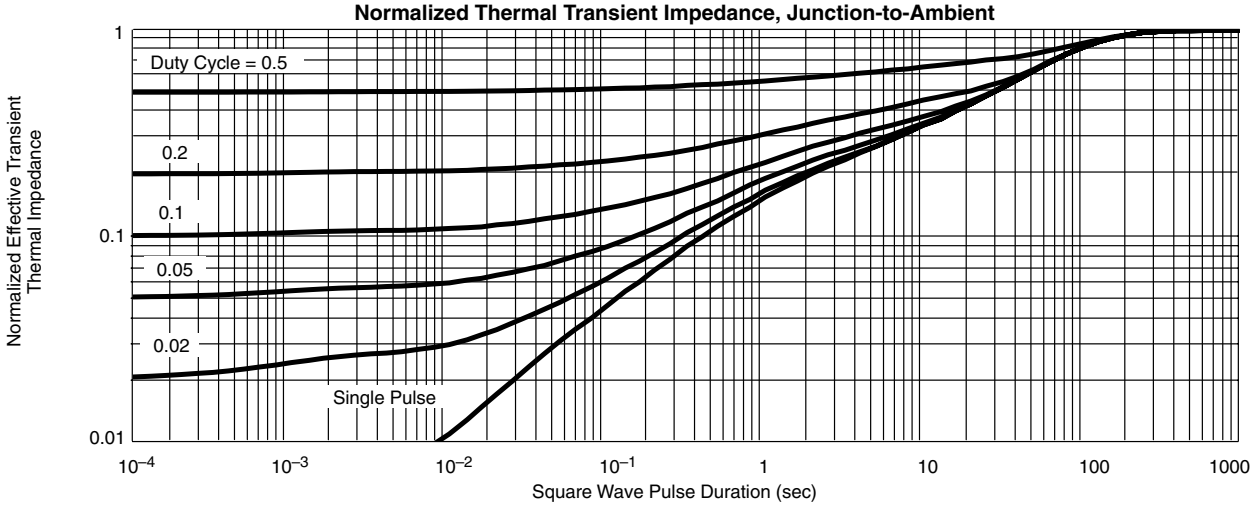




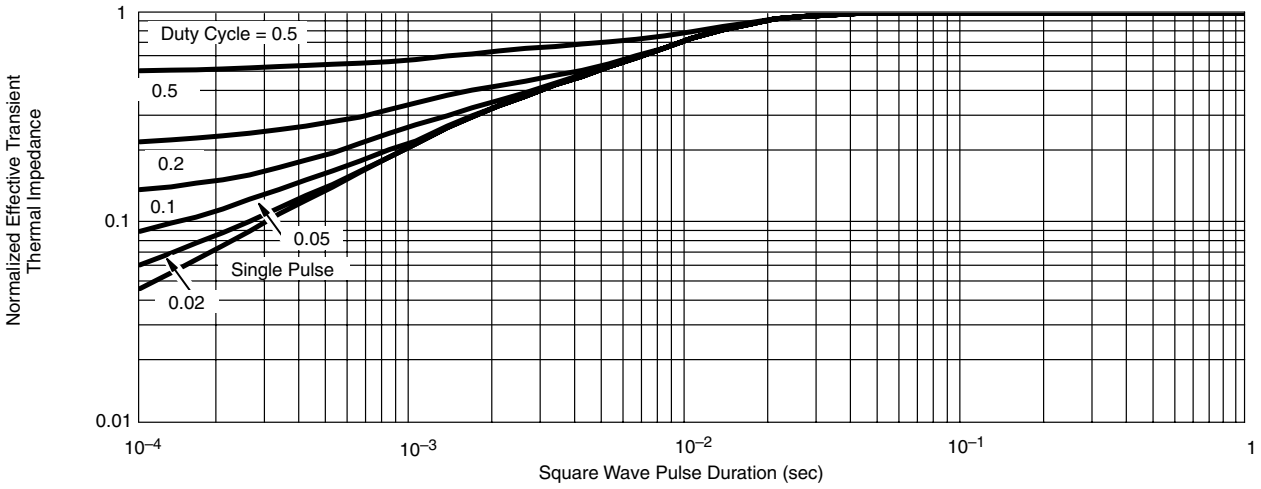
*The power dissipation P_D is based on $T_{J(max)}$ = 150°C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73530.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.